**Fully Differential Amplifier Power Stage**

By

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***1. Preliminary***

The goal of this publication is to attract the readers to investigate the possibility of fully differential amplifiers used to drive output stage power transistors.

Fully Differential Amplifiers are the preferable way to provide the signal for ADC and other audio purposes because of the advantages explained in <http://www.ti.com/lit/an/sloa054e/sloa054e.pdf>

There are two main types of fully differential amplifiers, classified by the supply voltage :

\* Low Supply Voltage : Ucc – Uee < = 12V

\* Normal Supply Voltage : Ucc – Uee < = 36V

The fully differential amplifiers with normal supply voltage are of interest. These can be classified into two categories by their slew rate and noise :

\* Normal Slew Rate ( ~ 50 V / us ), Extremely Low Noise ( ~ 1 nV / SQRT( Hz ) )

\* High Slew Rate ( ~ 650 V / us ), Very Low Noise ( ~ 4 nV / SQRT( Hz ) )

The noise below 10Hz can be filtered for audio applications.

The idea is to use fully differential amplifiers to control feedbacked transistors, ideally, without any resistors.

Non feedbacked, common collector buffer transistors cannot be used for high quality audio because their Ube becomes part of the signal and changes with the signal. Ube can change between 0.5V and 2V for power transistors. Changes between 0.5V and 1.5V are typical. When a center DC current is provided, one of the Ube’s increases while the other decreases which would be perfect provided they change the same either way, but they may not. Common emitters with a DC feedback and a centered quiescent current are OK.

All non feedbacked by an amplifier transistor circuits suffer from high non linearity which can only be corrected by the powerful feedback of an amplifier. The higher the slew rate and the transmission frequency, the better the nonlinearity. Slew rate is more important than transmission frequency because high output signals are expected.

Resistors create a delay with the transistor capacitors which can be in the range of fF (RF transistors ) to a few hundred pF ( power transistors ). The higher the power of the transistors, the higher the transistor capacitances Ccb, Cce and Cbc. Manufacturers of fast RF transistors would try to decrease Ccb in order to use the transistors for a common base current source to drive antenas and would not care much for Cce and Cbe, although some do. Most achieve low capacitances by a huge reduction in the maximum voltages Uce and Ube and thus Ucb. A Darlington which drives a low impedance load ( such as 4 Ohm speakers ) would act as a capacitance buffer. The low capacitance, low power transistor is charged by the source either directly or through a resistor, and the high power transistor is charged either through a resistor and the load or by the load only.

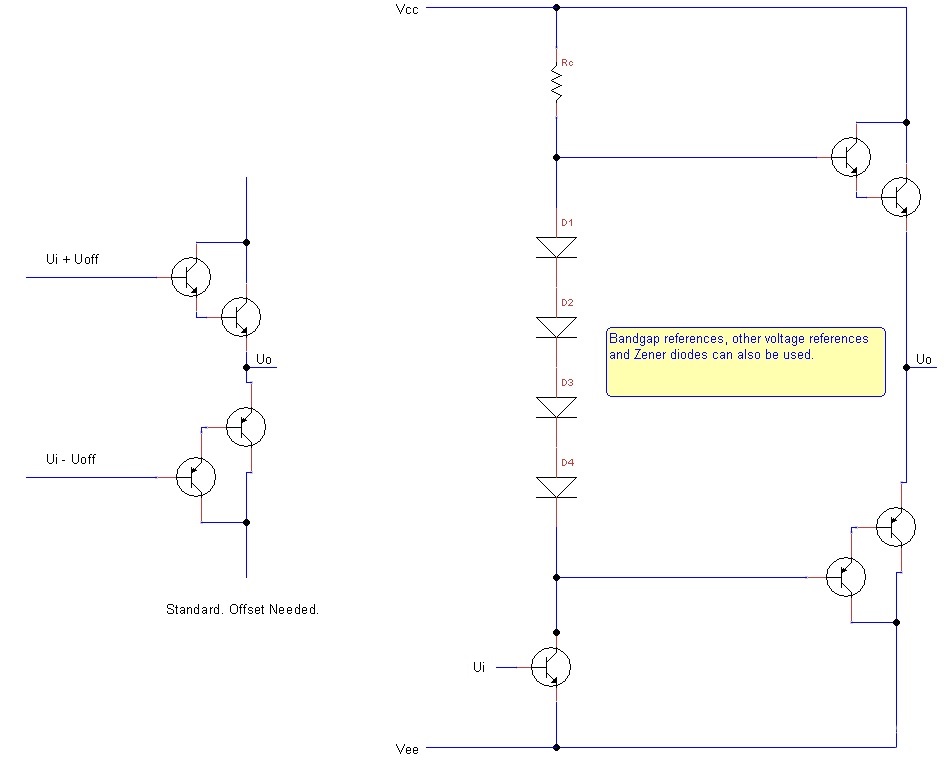
Common collectors’ Cbe’s is charged directly from the low output impedance and high current ( ~ 85mA ) of the amplifier, while their Cce is charged through the low impedance ( 4 Ohms ) of the load. Thus, directly connected common collectors are preferable where possible to be used.

When feedbacked or non feedbacked transistors with a center DC current, such as common emitters, their current circles around their DC offsets. Thus, their capacitances only introduce tiny delay which is not important. When they are feedbacked by an amplifier, the only requirement is the amplifier must be able to drive the transistor capacitors without oscillations, i. e. to handle the delay. Darlngtons and gain can be used to even increase the stability. In most cases, the amplifiers would be able to drive even the capacitance of non Darlngton’ed power transistors directly.

The problem is when the amplifiers have to jump as in the two common collector schematic ( the first one ) of the figure Output Offset. Many people wrongly think the amplifiers are too slow to make the jump quickly. The truth is the other way around : amplifiers are fast, transistors are slow. An high slew rate ***voltage feedback*** amplifier would have a typical slew rate of 650 V / us to 1200 V / us. Current feedback amplifiers would have much higher slew rates, yet, they are more susceptive to noise.

650 V / us = 0.65 V / ns. This means, without load capacitance, an amplifier can jump one nominal Ube for 1 ns and 4Ube ( 2.8V nominal ) for around 4ns. Ube is very low around 0V which makes the jump even faster.

The fastest audio signal is 20KHz with a half period of 25us. 4ns is negligible for the audio signals which are slow as compared to other signals in electronics. Even more : when the output signal is high, the effect of any negligible non linearities and distortions is even more negligible and will be mitigated even more by parasitic or non parasitic capacitances in the load ( speaker ).



***Figure : Output Offsets***

Figure Output Offsets shows the two common collector ( one for the positive and one for the negative waves ) and the typical solution with output offset provided by the diodes ( Zeners, bandgaps can be used too ) and the common emitter transistor which requires Rc which charges the positive, NPN common emitter and the Cce of the low power, common emitter transistor capacitances. This solution is good despite the resistor because of the Darlington capacitance buffer and the low Cce of the low power common emitter. Low noise RF transistors can be used for the first transistors of the Darlingtons as well as for the common emitters provided they can handle the typical 30V supply of the amplifier. ( Although there are ways to interface high voltage transistors to amplifiers, these schematics will not be examined here. At positive and negative 15V supply, the maximum RMS is around 10V which can provide 25W trough the output speaker which is sufficient for a lot of applications ).

Although the standard output offsets schematic suffices, the question is whether a different way of offset, an input offset can be used, so Rc does not affect the schematics and the common emitter transistor does not affect the linearity.

I have previously discussed some normal amplifier circuits such as two amplifier ( in *some* solutions with two amplifiers, beware of the saturation recovery which may be slow with *some* amplifiers ), thus the question I want to put for awareness is :

Can a solution can be found which :

1. Uses two common emitters only ( two Darlingtons or two transistors, the logical transistors are two in either case ) to keep the quiescent current through the transistors to around 0V and not to have DC center current.

2. The common emitters are feedbacked.

3. Provides such voltages to the common emitter bases, so when the input and output voltages are 0V, the voltage of the base of the NPN is around 0.7V when a single output transistor is used and around 1.4V when a double Darlington is used. For the PNP, these voltages are – 0.7V and – 1.4V. Thus, when Ui = 0V and Uo = 0V, Ubnpn = N \* 0.7V and Ubpnp = - N \* 0.7V where N is the number of transistors per Darlington and can be an integer value >= 1.

**Simply said, for Darlingtons :**

**When Ui = 0V and Uo = 0V,**

**Ubnpn ~ 1.4V**

***and***

**Ubpnp ~ 1.4V**

***and***

**1.4V offsets are independently provided**, so they can be adjusted as per the design ( may be lower than the lowest Ube of a Darlington or slightly higher than the highest where some tiny quiescent current is used just to keep the transistors close to closed but not fully closed ).

There are easy ways to use common emitters or one common emitter, one common collector at the output but there would be current at 0V and non linear run of the amplifier’s outputs which may introduce even more nonlinearity error than a direct, non ofsetted jump.

In other words, a schematic is needed to provide :

Ubnpn = G \* Ui + Goff \* Uoff

and

Ubpnp = G \* Ui – Goff \* Uoff

or

Ubnpn = - G \* Ui + Goff \* Uoff

and

Ubpnp = - G \* Ui – Goff \* Uoff

Logically, this is simplified to :

Ubnpn = Ui + Uoff

and

Ubpnp = Ui – Uoff

Simply said :

**Provide the same signal voltage to the bases of the NPN and PNP transistors ( or Darlingtons ) and opposite offsets.**

To achieve this a strange animal amplifier which has never been made with these parameters is needed :

The amplifier would have these logical input :

**Input Signal 1**

**Input Signal 1**

**Offset 1**

**Offset 2**

and these logical outputs :

**Output Signal 1 = Input Signal 1 + Offset 1**

**Output Signal 2 = Input Signal 2 + Offset 2**

and

**Two Feedbacks ( Gains OK Too ) Possibility.**

This can be simplified to :

and

**Input Signal**

**Offset**

and

**Output Signal 1 = Input Signal + Offset**

**Output Signal 2 = Input Signal – Offset**

and

**Two Feedbacks ( Gains OK Too ) Possibility.**

An idea is to have three independent feedbacks : one for the signal which is taken from the output and delivered to the signal input and one for each offset. Two are also possible one for each signal inputs when two of these are used and none for the offsets or one for the signal input ( when one is used ) and one for the two offsets. One is also possible : one for the single signal input ( the two outputs are reciprocal but the two of them must be included in the single signal feedback ) and none for the offsets.

*The needed amplifier is the opposite of the fully differential amplifier and may be possible to be accomplished by standard amplifier and or by transistors but the question is :*

**Can this be accomplished by a fully differential amplifier?**

**Please, do inform and correct.**

***Of course, to make the whole amplifier from either IC amplifiers or transistors only or the two thereof is always a good idea. The question is whether something can be achieved with whatever is available.***

***2. Some Schematics***

Some schematic ideas will be published, some now, others, in a while.

First, the basic principles of a fully differential amplifier, from which a schematic with a fully differential amplifier can be fully derived are :

**1. No current flows into inputs**

**2. Vp = Vn : positive amplifier input is equal to negative amplifier input when physically possible ( negative feedback is required )**

**3. Uo+ + Uo- = 2 \* Uocm : sum of positive amplifier output and negative amplifier output is equal to the double of the OCM input**

**4. Point 2 depends on external components, i. e. is EXTERNAL. Point 3 is :**

**\* done internally, i. e. INTERNAL**

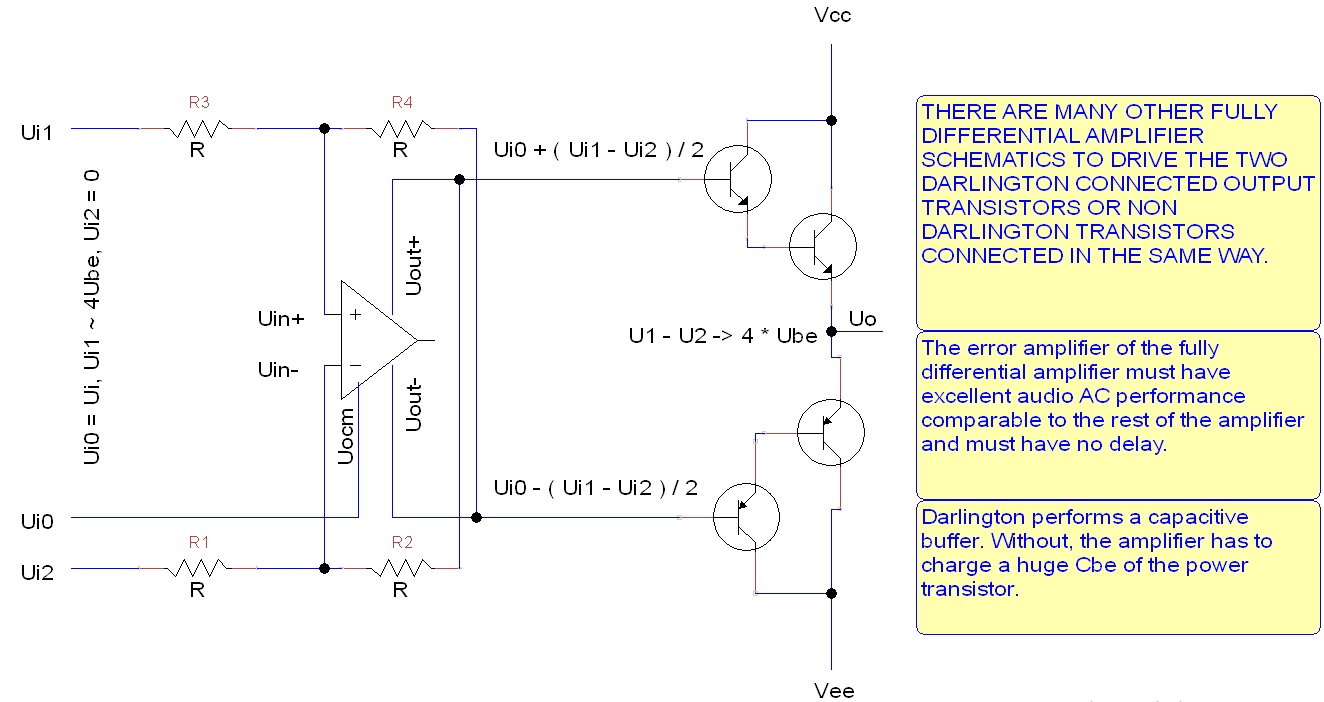
**\* independent of external components**

**\* independent of the positive and negative input signals**

**\* independent of any inputs, outputs and signals, except OCM, i. e. Uocm is an offset voltage**

Point 1 and 2 are the same for the normal amplifier and they are sufficient for the normal amplifier. Point 1 and 2 are the same for the differential amplifier BUT are insufficient. Poin 3 and 4 are needed.

***2.1 No Feedback Schematic***



***Figure : Fully Differential Amplifier No Feedback***

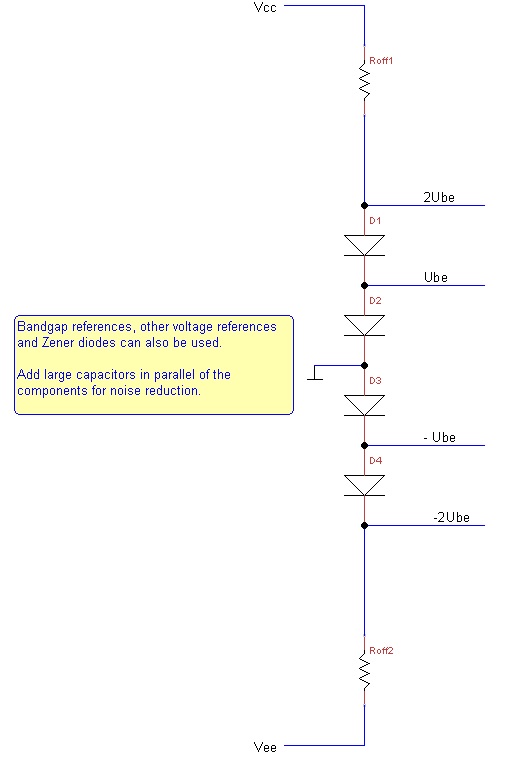
The amplifier outputs Ui + Uoff and Ui – Uoff. When Ui = 0, the amplifier outputs Uoff and – Uoff. Uoff can be made to be around 2Ube, thus, the transistors will not be closed ( or will not be fully closed ) when Ui = 0.

Problems :

1. The transistors are not feedbacked.

2. The feedback amplifier built inside of the fully differential amplifier ( called error amplifier ) must be of audio quality and not DC.

Input offset can be provided in many ways.

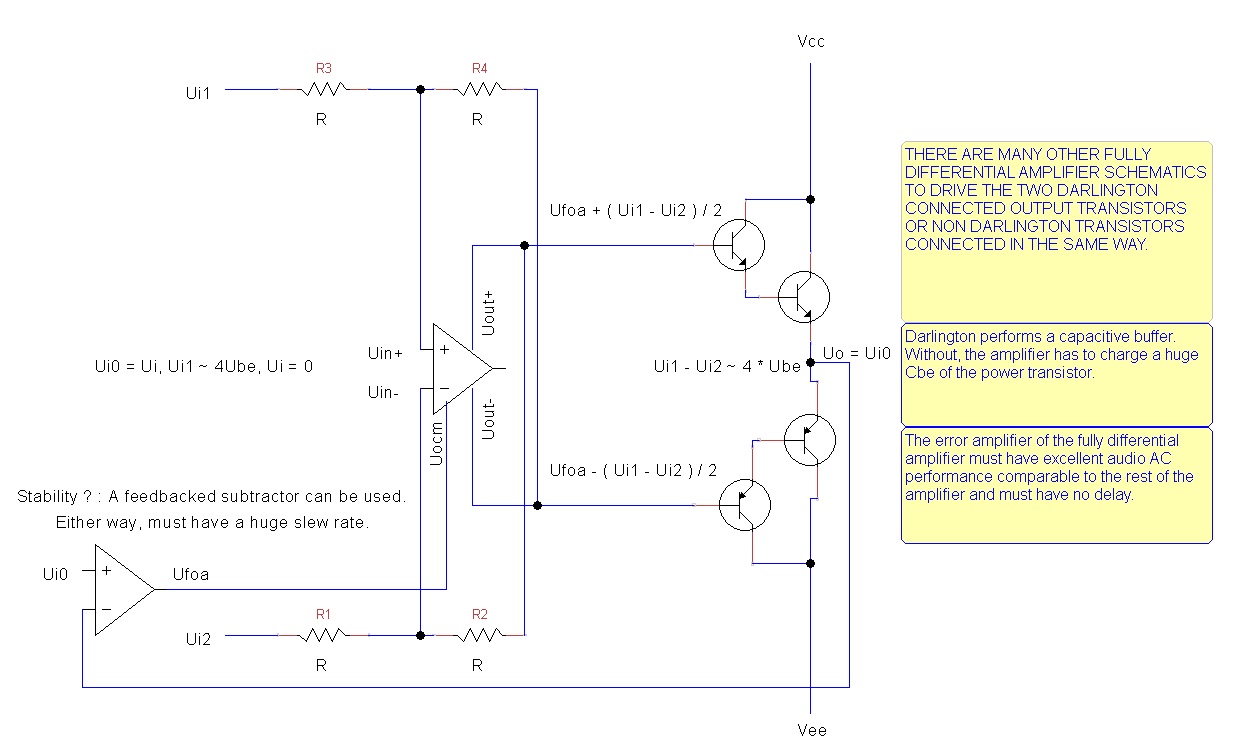


***Figure : Input Offsets***

When ground is disconnected and reconnected where the sign – 2Ube is, there will be 4Ube at the upper output.

There are 2.0V, 2.4V and 2.7V Zeneres which can be used too. A Zener and a diode would provide temperature stability.

***2.2 Fully Differential Amplifier Power Stage with External Feedback***



***Figure : Fully Differential Amplifier Power Stage with External Feedback***

The second amplifier ensures Uo = Ui. Higher Uo brings a lower Ufoa which brings lower Uo, therefore the overall feedback is negative.

When Ui = 0, Uo = 0 and Ufoa = 0. Then the amplifier will output Uoff and -Uoff ( independent of Uocm ) which can be adjusted to be 2Ube and – 2Ube.

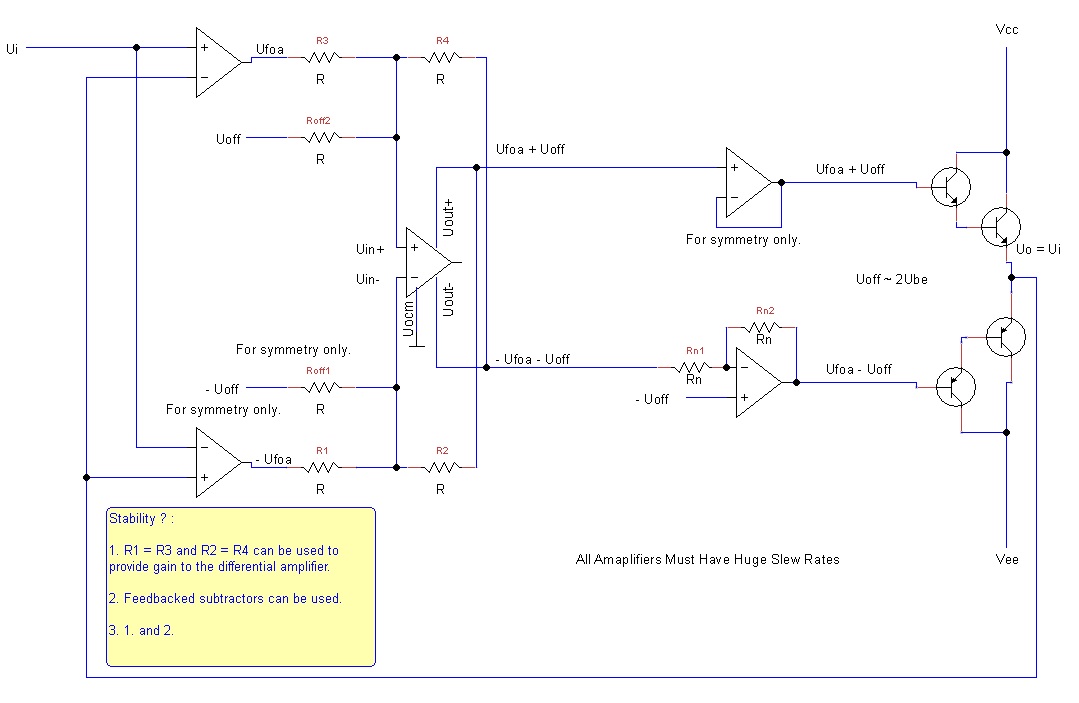
Problems :

1. The feedback amplifier built inside of the fully differential amplifier ( called error amplifier ) must be of audio quality and not DC.

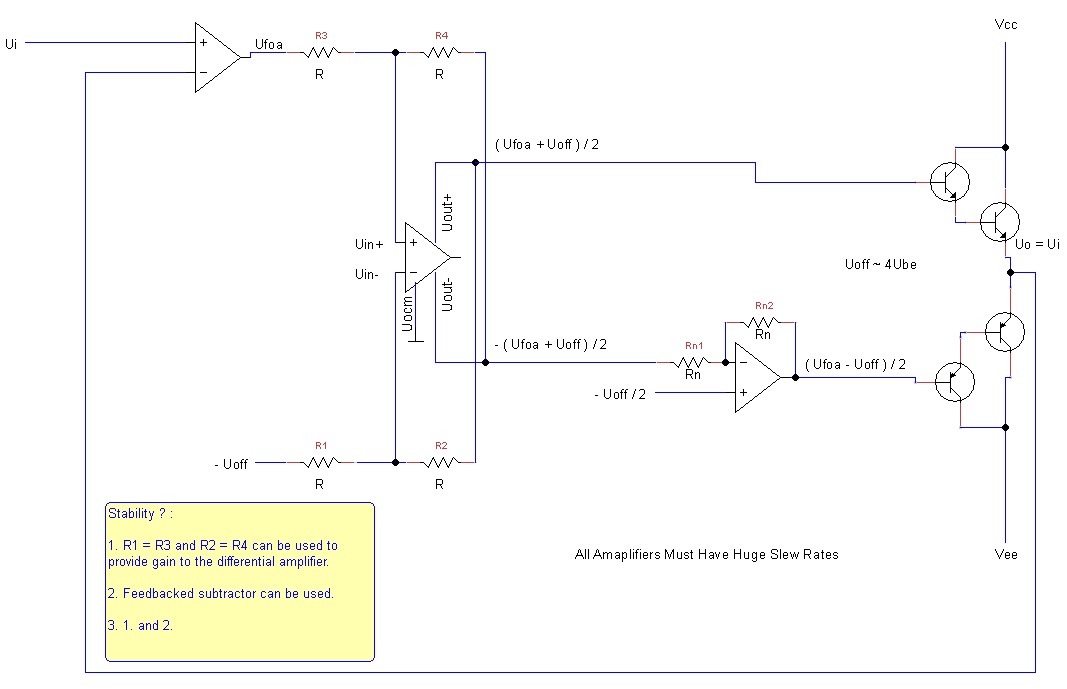
2. A second high quality, fast normal ( not fully differential ) amplifier is needed.

Because the built in feedback amplifier ( error amplifier ) is not believed to be of audio quality and with a huge slew rate, external amplifier solutions have been sought. They all provide offset to the transistors when Ui = Uo = 0 and only around 0 the two transistors will be close to open or slightly open. When the signal is big, the slope is steep and the transistors may be slow to open or almost to open but then the nonlinearity error caused by the jump is low anyway ( because the amplitude is big ). When the signal is low, the nonlinearity error caused by the jump is bigger but then the slope is shallow and the transistors should be able to open or almost open ( depends on the Uoff ). Here are some schematics. More simplification and many combinations can be played based on the idea of these and the principles of work of the fully differential amplifier.

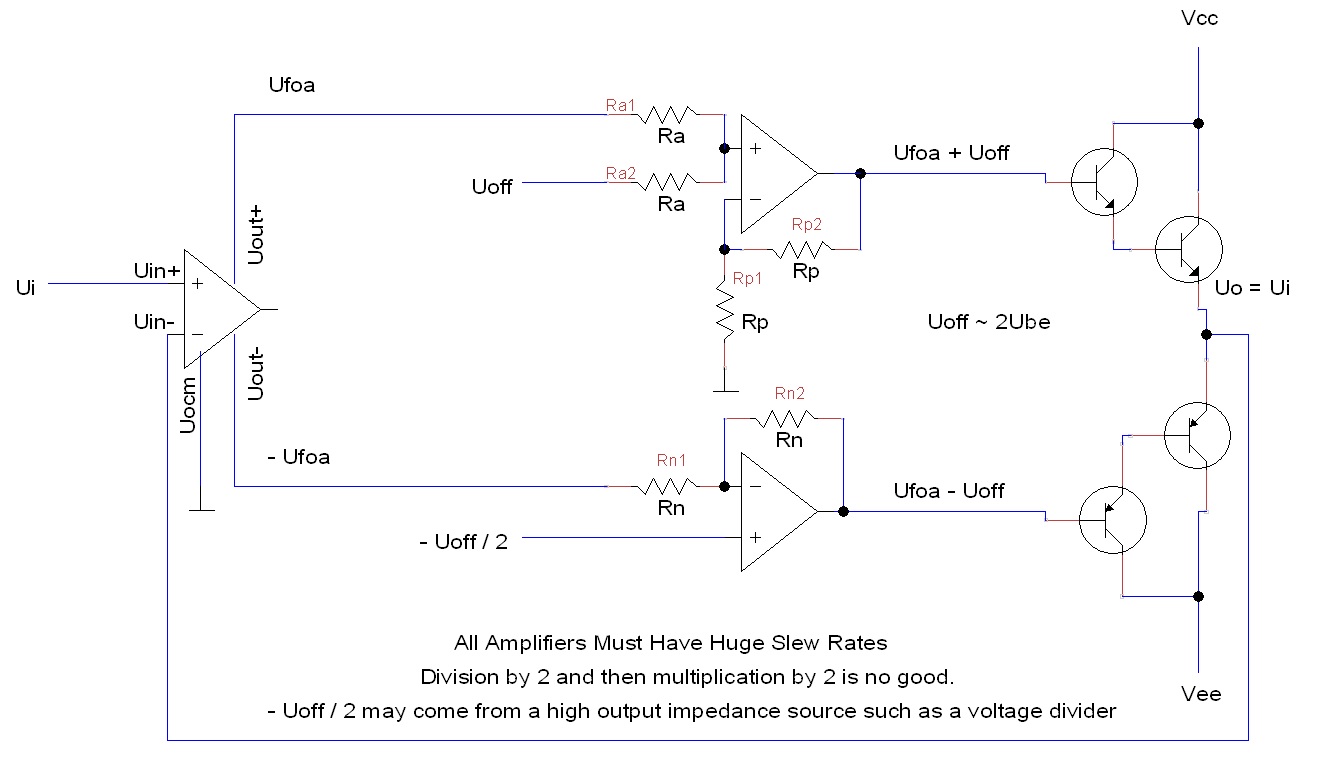
Basically, these schematics give offset to the bases of the transistors ( output offset ) and or or modify ( negate, repeat, amplify ) the two outputs of the fully differential amplifier. The idea is similar to the standard output offset arrangement discussed here too but there are no any resistors to delay the transistors’ parasitic capacitors and the job to handle these parasitic capacitor is given to amplifiers which, unlike resistors and transistors, are super fast with huge slew rates of 650 to 1200 V / us for voltage feedback audio amplifiers.



***Figure : Fully Differential Amplifier Power Stage with External Feedback with Two Input Amplifiers***



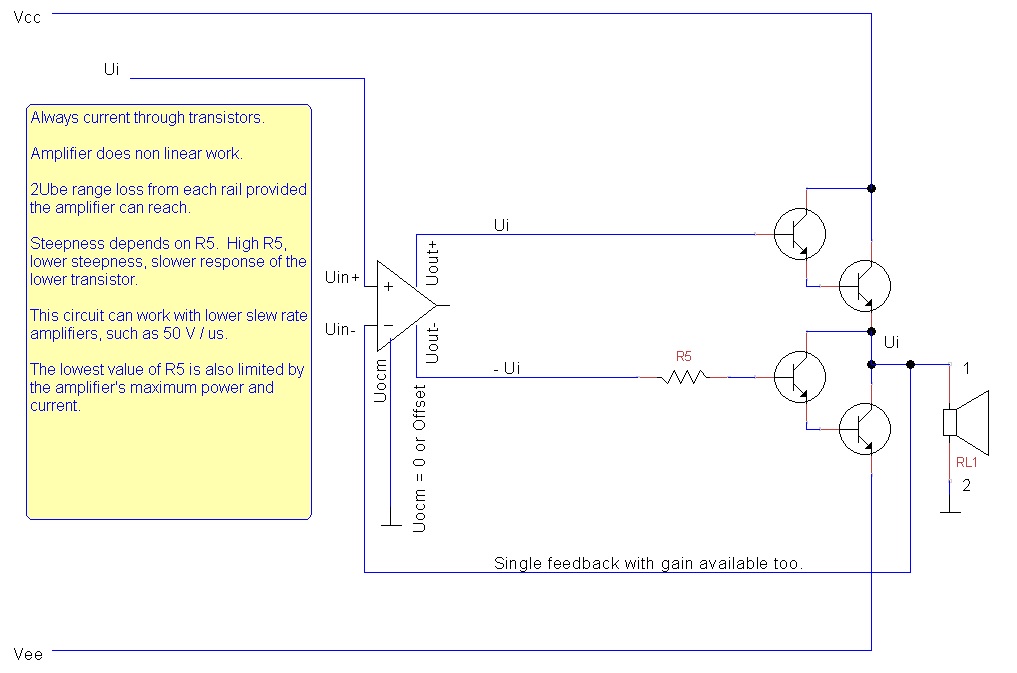
***Figure : Fully Differential Amplifier Power Stage with External Feedback with Two Input Amplifiers, Simplified***



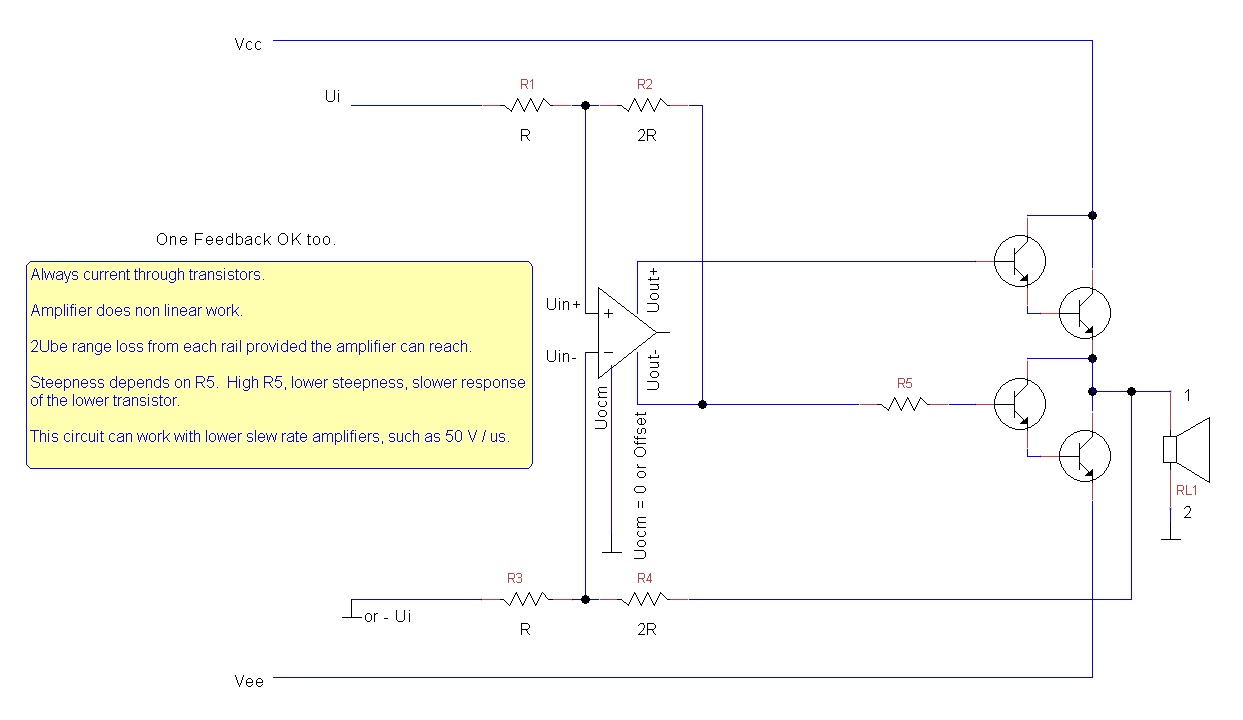
***Figure : Fully Differential Amplifier Power Stage with External Feedback with Two Input Amplifiers, More Simplified***

***2.3 Fully Differential Amplifier with Common Emitter and Common Collector***

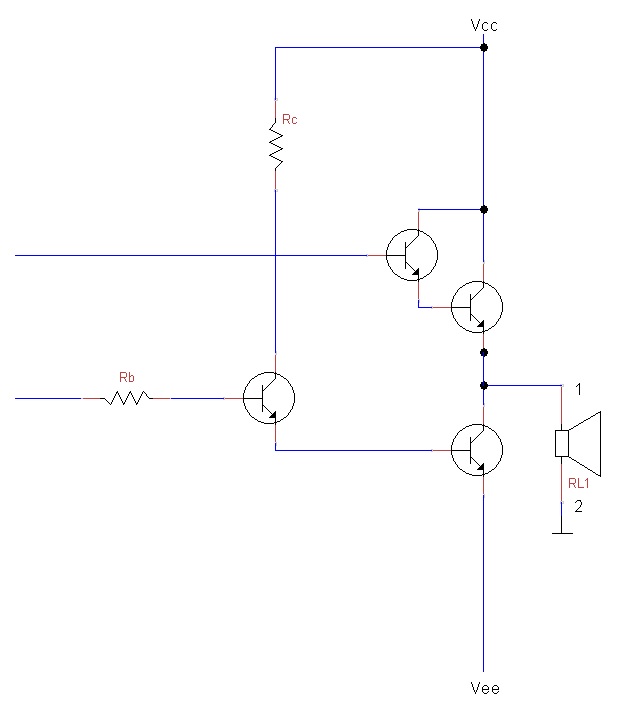
Depicted are schematics for common collector with common emitter arrangements. Different output transistor configurations are provided. The figure called : Output Transistors, Common Emitter, Collector and Common Collector, Collector may be of interest.



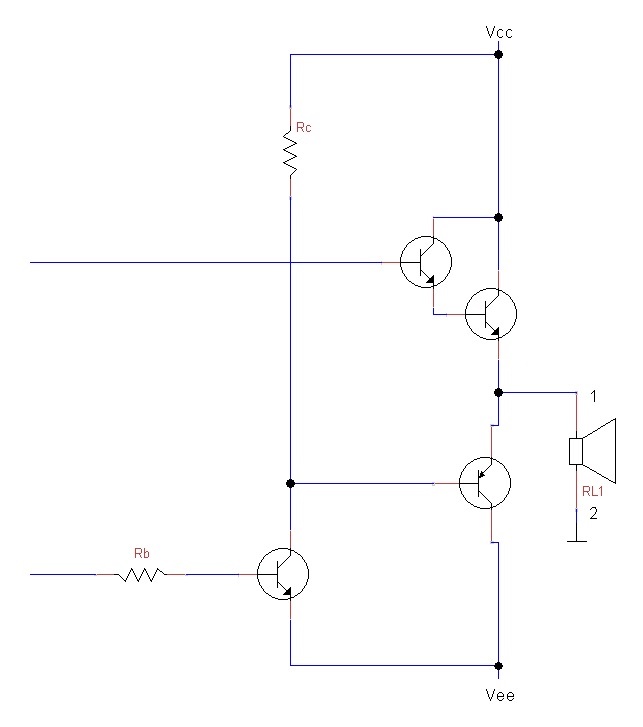
**Figure : Fully Differential Amplifier Power Stage, Common Emitter and Common Collector with One Feedback**



**Figure : Fully Differential Amplifier Power Stage, Common Emitter and Common Collector with Two Feedbacks**



**Figure : Output Transistors, Common Emitter, Emitter and Common Collector, Collector**

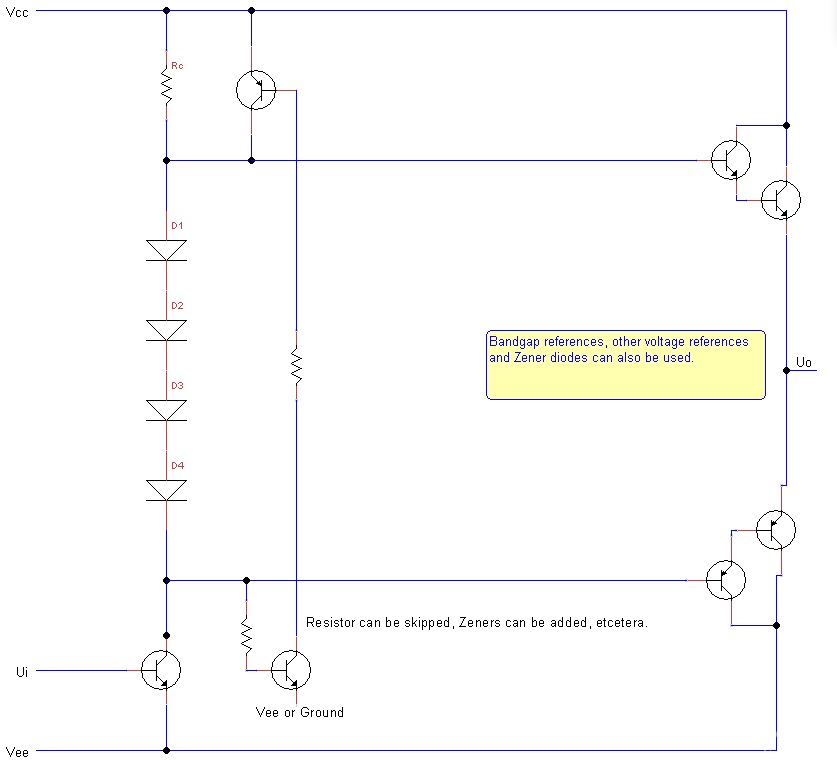


**Figure : Output Transistors, Common Emitter, Collector and Common Collector, Collector**

***3. Some Standard Applications of the Fully Differential Amplifier***

***3.1. Compensations of the Common Emitter Collector Resistor in the Output Offsets Circuit***

The collector resistor, as mentioned, slows down the performance and, even, in some cases, may not provide the necessary current to the output common emitter. Thus, the idea is to shunt this resistor when the common emitter voltage is positive. The compensation can be adjusted to perform in any level by resistors, Zeners, diodes, etcetera. The use of a Zenner or diodes ( which ac like a Zener ) is encouraged to start at a positive voltage of the common emitter chain. Thus, the resistor is not shunt when the common emitter provides a negative voltage where the transistor is more open. The common emitter transistor will be able to provide lower resistance for the capacitors of the power common collector negative wave transistor. When the common emitter voltage is high, i. e. the common emitter transistor is not so much open, at higher positive voltages, the resistor can be shunt for a faster charge of the positive common collector power transistor capacitors as well as for a higher base current to the same.



***Figure : Output Offsets with Two Transistor Compensation***

**3.2 Standard Non Standard Circuits**

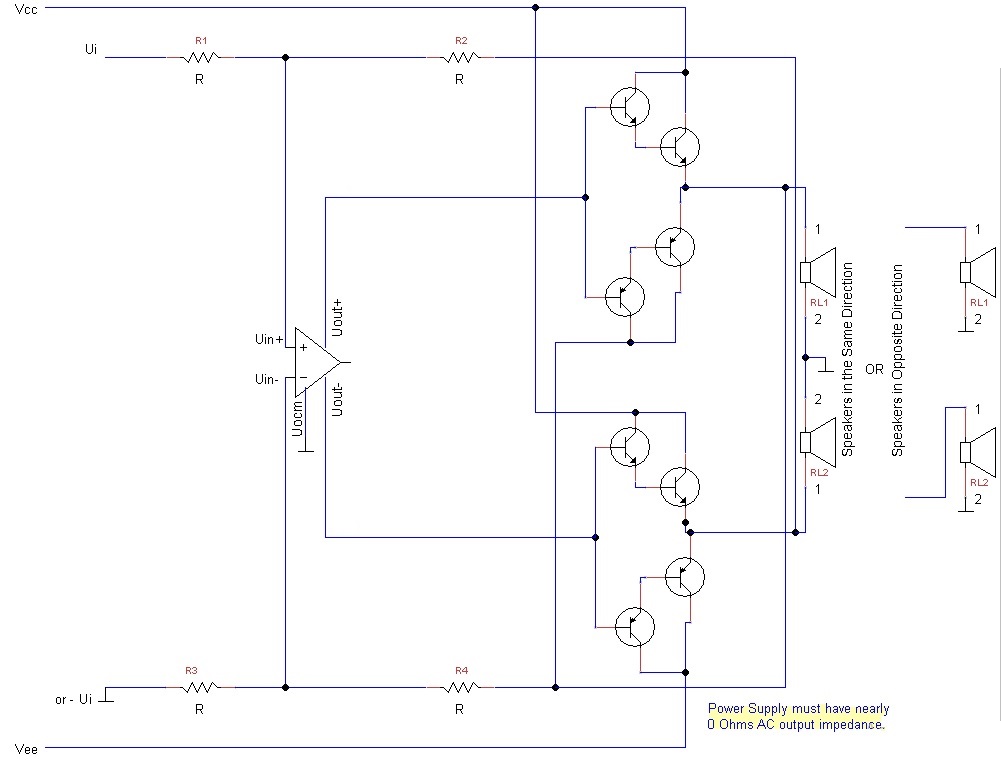
These use two speakers per channel for which the differential amplifier proves to be suitable. For mono, two speakers are needed. For stereo : four.

Each of the outputs of the differential amplifier controls a speaker. In most circuits, only the standard, direct transistor connection is shown. The output offset transistor connections can be used there too. However, the idea is mainly to show how two speakers can be used with one fully differential amplifier. *This is not very practical and will probably never be used but is interesting.*

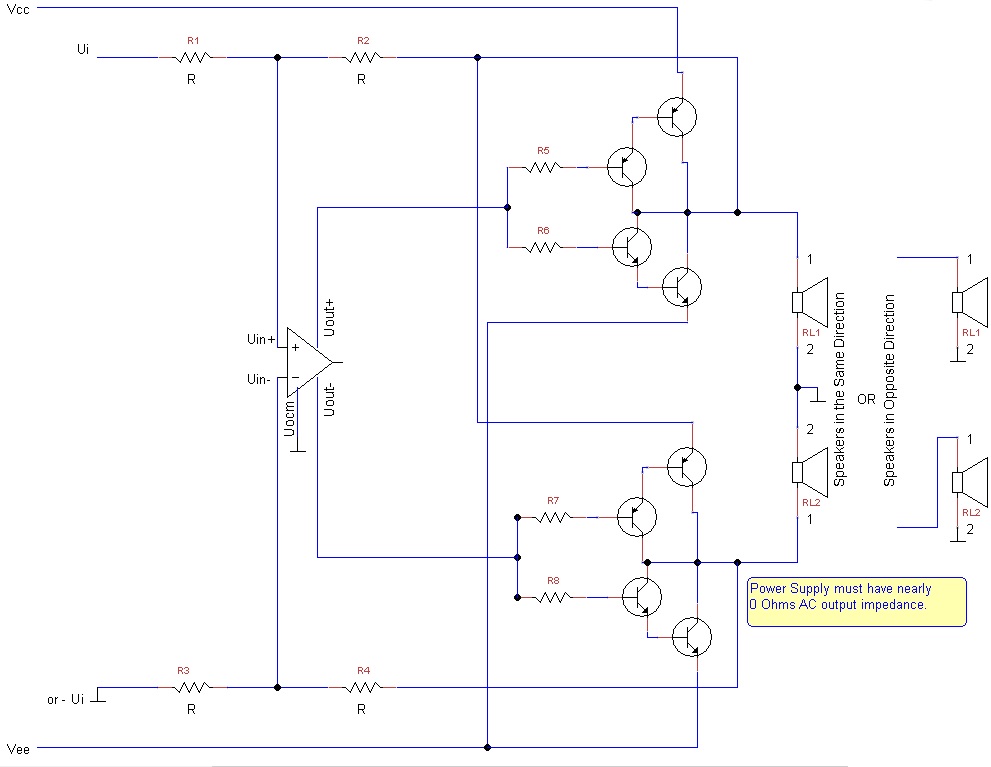
The speakers can be controlled either in phase or in opposite ( 90 degree shift ) phases.

When the speakers are controlled in phase, there is no difference in their outputs : when speaker one blows, speaker two blows too, when speaker one sucks, speaker two sucks too. These can be positioned next to each other.

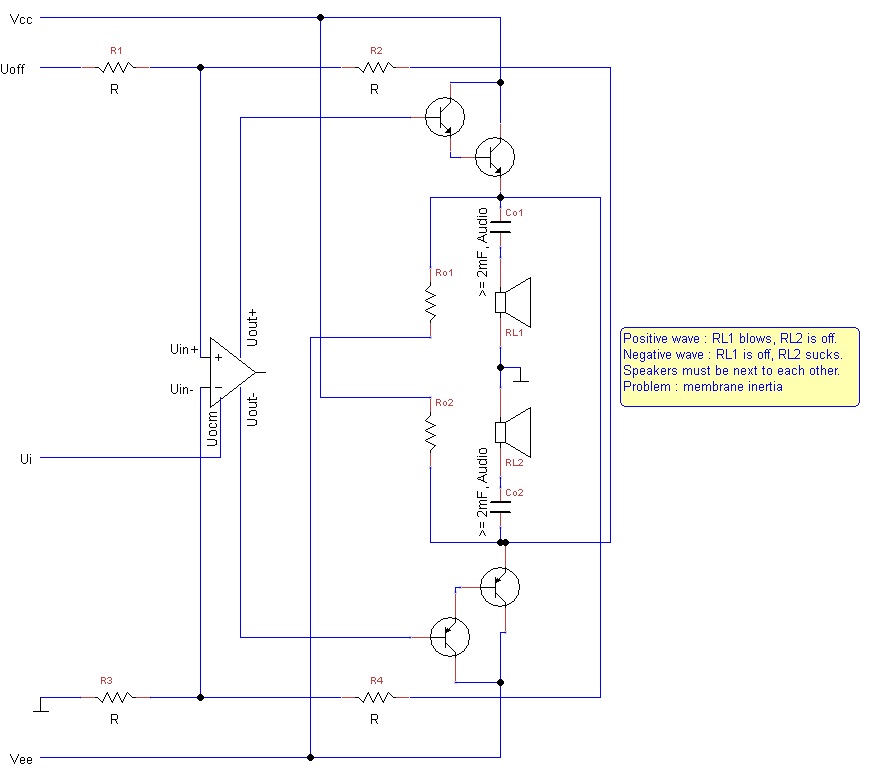
When the speakers are controlled in opposite phases, when speaker one blows, speaker one sucks and when speaker one sucks, speaker two blows. These can be positioned against each other. This will give an even flow of the air.



***Figure : Fully Differential Amplifier Power Stage, Standard with Two Speakers per Channel***



***Figure : Fully Differential Amplifier Power Stage, Common Emitters with Two Speakers per Channel***



***Figure : Fully Differential Amplifier Power Stage One Speaker per Half Wave***

This is strange : each of the speakers work only with one half of the wave, upper with positive, lower with negative. They nearly do not display any sound ( or extremely quiet ) during non working wave.

***4. Some Ideas***

***4.1. Square Wave Offset***

A square wave offset can be provided elsewhere in the circuit. A fast comparator compares Ui with 0 and generates a square wave with amplitude Uoff. So, Uoff changes signs and this is necessary. The comparator must be very fast and must not go to saturation or must have a fast saturation recovery or be externally and or internally protected from saturation.

***4.2. Invertor***

An invertor with huge slew rate can be put after Uo- with or without a local feedback. This invertor drives the PNP buffer ( s ).

*To keep the symmetry, one non feedbacked, huge slew rate amplifier can be put after Uo+. The positive input is connected to Uo+, the negative : to ground. The output : to the base of the common collector Darlington NPN. Another non feedbacked, huge slew rate amplifier can be put after Uo-. The positive input is connected to ground, the negative : to Uo-. The output : to the base of the common collector PNP Darlington.*